Hardware-Software Co-Design for Next Generation Dark Silicon Multimedia Systems

Muhammad Usman Karim Khan (Ph.D. Candidate), muhammad.khan@kit.edu
Jörg Henkel (Advisor), Muhammad Shafique (Research Group Lead)

Introduction and Challenges

- High complexity multimedia systems (image/video processing) under throughput constraints
- Meet applications’ performance requirements — parallelization, accelerators, etc.
- Dark silicon — power/thermal constraints for many-core and multi-threaded workloads
- Increased energy/power efficiency (prolonged battery lifetime)
- Increase reliable life-time (reduced aging rate of the on-chip SRAM video memory)

Required

- Runtime synergistic optimization of application and hardware parameters
- Explore hardware-software co-design and co-optimization space
- Fully exploit complexity, power, and resource-saving and reliability improvement by jointly considering software and hardware layers

Our Novel Contributions

- CES265: C-based, multithreaded, High Efficiency Video Coding (HEVC) software
- One thread is ~13.2x than the reference HEVC encoding software (HM-9.2)
- SRAM Aging Analysis and Visualization Software
- GUI-based (written in C#) memory aging analysis tool
- Fast evaluation of anti-aging techniques and visualizations (heatmaps, graphs etc.)
- H.264 VHDL (for Altera Arria II GX260 FPGA) — Mid of July, 2015

Conclusion

- Application- and resource-aware hardware-software co-design
- Account for the next generation thermal design power constraints and reliability consideration at both software and hardware layers
- Enables system design and characterization, by determining the degree of parallelism, amount of task offload and resource/power budgeting at runtime
- Methodologies for distributed power-efficient accelerator design, and its scheduling of loosely coupled accelerators in a many-core system
- Novel scratchpad design methodology, with aging resilience

List of Publications